

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	10623101
Filing Date	2003-07-18
First Named Inventor	Guillermo Rozas
Art Unit	2183
Examiner Name	Petranek, Jacob Andrew
Attorney Docket Number	TRAN-P072

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NON-PATENT LITERATURE DOCUMENTS

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	2	Ozer et al., A Fast Interrupt Handling Scheme for VLIW Processors, October 12-18, 1998, Proceedings of International Conference on Parallel Architectures and Compilation Techniques, Pages 136-141	<input type="checkbox"/>
	3	TITLE: A VLIW architecture for a trace scheduling compiler, author: Colwell et al, ACM, 1987	<input type="checkbox"/>
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	7	TITLE: RISC II: a reduced instruction set VLSI computer, author: Patterson, ACM, 1998	<input type="checkbox"/>
	8	FINAL OFFICE ACTION DATED 6-25-03; PATENT NO.: 6738892; TRAN-P021	<input type="checkbox"/>

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9	NON-FINAL OFFICE ACTION DATED 4-11-02; PATENT NO.: 6738892; TRAN-P021	<input type="checkbox"/>
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18	NON FINAL OFFICE ACTION DATED 9-24-07; 10/672,790; TRAN-P243	<input type="checkbox"/>
19	ISSUE NOTIFICATION DATED 5-18-04; PATENT NO.: 6738892; TRAN-P021	<input type="checkbox"/>

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